

## CLAIM LISTING

1. (Previously Presented) A communications bus connected between a source node and a destination node, the communications bus including:
  - (a) a number of alternate transmission paths extending between the source node and the destination node on a common substrate comprising a semiconductor chip;
  - (b) a source switching arrangement interposed between the source node and the alternate transmission paths, the source switching arrangement being operable to selectively connect the source node to a selected one of the alternate transmission paths and disconnect the source node from each other alternate transmission path; and
  - (c) a destination switching arrangement interposed between the destination node and the alternate transmission paths, the destination switching arrangement being operable to selectively connect the destination node to the selected one of the alternate transmission paths and disconnect the destination node from each other alternate transmission path.
2. (Original) The communications bus of Claim 1 wherein:
  - (a) the source switching arrangement includes multiple source switching devices, a different source switching device connected between the source node and each alternate transmission path; and
  - (b) the destination switching arrangement includes at least one destination switching device connected between the destination node and each alternate transmission path.

1       3. (Original) The communications bus of Claim 1 wherein:

2           (a) the different source switching devices include at least one multiplexer; and

3           (b) the at least one destination switching device comprises a multiplexer.

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5       4. (Original) The communications bus of Claim 1 further including:

6           (a) a source switch control structure for controlling the operation of the source

7              switching arrangement; and

8           (b) a destination switch control structure for controlling the operation of the

9              destination switching arrangement.

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11      5. (Previously Presented) The communications bus of Claim 4 wherein the source switch

12      control structure and the destination switch control structure each includes a nonvolatile

13      or volatile memory structure.

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15      6. (Original) The communications bus of Claim 1 further including test circuitry connected

16      to the source node and destination node for applying a test signal to each alternate

17      transmission path and for monitoring the destination node to determine whether the

18      respective test signal is properly received at the destination node.

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20      7. (Original) The communications bus of Claim 1 wherein:

21           (a) a receive node and first direction control node are associated with the source node,

22              and a send node and second direction control node are associated with the

23              destination node;

- 1                   (b) a send switching arrangement is interposed between the send node and each  
2                   alternate transmission path;
- 3                   (c) a receive switching arrangement is interposed between each alternate transmission  
4                   path and the receive node;
- 5                   (d) a first direction control switching arrangement is interposed between the first  
6                   direction control node and a control input of a tri-state driver associated with the  
7                   source node; and
- 8                   (e) a second direction control switching arrangement is interposed between the  
9                   second direction control node and a control input of a tri-state driver associated  
10                  with the send node.

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12       8. (Original) The communications bus of Claim 1 wherein:

- 13                   (a) the communications bus is also connected between a number of additional source  
14                   nodes and the same number of additional destination nodes;
- 15                   (b) a number of additional alternate transmission paths extend between each  
16                   additional source node and each additional destination node;
- 17                   (c) the source switching arrangement is also interposed between each additional  
18                   source node and the respective alternate transmission paths associated with that  
19                   respective additional source node, the source switching arrangement also being  
20                   operable to selectively connect each respective additional source node to a  
21                   selected one of the additional alternate transmission paths associated with that  
22                   source node and disconnect each respective additional source node from each  
23                   other additional alternate transmission path associated with that additional source  
24                   node; and

(c) the destination switching arrangement is also interposed between each additional destination node and the respective alternate transmission paths associated with that additional destination node, the destination switching arrangement also being operable to selectively connect each respective additional destination node to the selected one of the alternate transmission paths associated with that additional destination node and disconnect the respective additional destination node from each other additional alternate transmission path associated with that additional destination node.

11 arrangement comprises a number of multiplexers.

13 10. (Original) The communications bus of Claim 9 wherein the source node and number of  
14 additional source nodes are arranged side-by-side and wherein at least one pair of  
15 adjacent source nodes in this side-by side arrangement share a common multiplexer  
16 included in the number of multiplexers.

18 11. (Original) The communications bus of Claim 8 wherein:

19 (a) the source switching arrangement includes a first switching subset connected to a  
20 first subset of the alternate transmission paths;  
21 (b) the source switching arrangement further includes a second switching subset  
22 connected to a second subset of the alternate transmission paths; and

(c) the alternate transmission paths making up the second subset of alternate transmission paths are interleaved with the alternate transmission paths making up the first subset of alternate transmission paths.

12. (Original) The communications bus of Claim 8 wherein:

- (a) the source node and each additional source node is associated with a respective receive node and first direction control node, and the destination node and each additional destination node are associated with a respective send node and second direction control node;
- (b) a send switching arrangement is interposed between the send nodes and the alternate transmission paths;
- (c) a receive switching arrangement is interposed between the alternate transmission paths and the receive nodes;
- (d) a first direction control switching arrangement is interposed between the first direction control nodes and a control input of a number of tri-state drivers, each driver associated with a respective source node; and
- (e) a second direction control switching arrangement is interposed between the second direction control nodes and a control input of a number of additional tri-state drivers, each additional tri-state driver associated with a respective send node.

13. (Previously Presented) A communications bus connected between a number of source nodes and an equal number of destination nodes, the communications bus including:

- 1                   (a) a number of alternate transmission paths extending between each respective  
2                   source node and a matched one of the destination nodes on a common substrate  
3                   comprising a semiconductor chip, the matched destination node being matched to  
4                   a respective one of the source nodes;
- 5                   (b) a source switching arrangement, the source switching arrangement being  
6                   interposed between each respective source node and the respective alternate  
7                   transmission paths associated with that respective source node, the source  
8                   switching arrangement also being operable to selectively connect each respective  
9                   source node to a selected one of the alternate transmission paths associated with  
10                  that source node and disconnect each respective source node from each other  
11                  alternate transmission path associated with that source node; and
- 12                  (c) a destination switching arrangement, the destination switching arrangement being  
13                  interposed between each respective destination node and the respective alternate  
14                  transmission paths associated with that respective destination node, the  
15                  destination switching arrangement also being operable to selectively connect each  
16                  respective destination node to the selected one of the alternate transmission paths  
17                  associated with that destination node and disconnect the respective destination  
18                  node from each other alternate transmission path associated with that destination  
19                  node.

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21       14. (Original) The communications bus of Claim 13 wherein the source switching  
22                  arrangement comprises a number of multiplexers.  
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1       15. (Original) The communications bus of Claim 14 wherein the source nodes are arranged  
2                  side-by-side and wherein at least one pair of adjacent source nodes in this side-by side  
3                  arrangement share a common multiplexer included in the number of multiplexers.

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5       16. (Original) The communications bus of Claim 13 wherein:

6                  (a) the source switching arrangement includes a first switching subset connected to a  
7                          first subset of the alternate transmission paths;  
8                  (b) the source switching arrangement further includes a second switching subset  
9                          connected to a second subset of the alternate transmission paths; and  
10                 (c) the alternate transmission paths making up the second subset of alternate  
11                          transmission paths are interleaved with the alternate transmission paths making up  
12                          the first subset of alternate transmission paths.

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15       17. (Original) The communications bus of Claim 13 wherein:

16                  (a) each source node is associated with a respective receive node and first direction  
17                          control node, and each destination node is associated with a respective send node  
18                          and second direction control node;  
19                  (b) a send switching arrangement is interposed between the send nodes and the  
20                          alternate transmission paths;  
21                  (c) a receive switching arrangement is interposed between the alternate transmission  
22                          paths and the receive nodes;

1                   (d) a first direction control switching arrangement is interposed between the first  
2                   direction control nodes and a control input of a number of tri-state drivers, each  
3                   driver associated with a respective source node; and

4                   (e) a second direction control switching arrangement is interposed between the  
5                   second direction control nodes and a control input of a number of additional tri-  
6                   state drivers, each additional tri-state driver associated with a respective send  
7                   node.

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9       18. (Previously Presented) A method for compensating for errors in a communications bus  
10                  between a source node and a destination node, the bus including alternate transmission  
11                  paths between the source and destination node on a common substrate, the method  
12                  including the steps of:

13                  (a) applying a test signal to a first one of the alternate transmission paths between the  
14                  source node and the destination node;

15                  (b) determining whether the test signal is properly received at the destination node;  
16                  and

17                  (c) if the test signal is not properly received at the destination node, switching to a  
18                  second one of the alternate transmission paths between the source node and  
19                  destination node.

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21       19. (Original) The method of Claim 18 further including the steps of:

22                  (a) applying a second test signal to the second one of the alternate transmission paths  
23                  between the source node and the destination node; and

1                   (b) determining whether the second test signal is properly received at the destination  
2                   node.

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4       20. (Original) The method of Claim 18 wherein the communications bus extends between a  
5                   number of source nodes and a like number of destination nodes, and the bus includes a  
6                   number of alternate transmission paths between each source node and a respective one of  
7                   the destination nodes, and wherein the method further includes:

8                   (a) applying a respective test signal to each alternate transmission path between each  
9                   respective source node and its respective destination node;  
10                  (b) determining whether each respective test signal is properly received at the  
11                   respective destination node; and  
12                  (c) for each respective test signal that is not properly received at the respective  
13                   destination node, switching the respective source node to a different one of the  
14                   alternate transmission paths between the respective source node and destination  
15                   node.

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17       21. (Original) The method of Claim 20 wherein the step of switching the respective source  
18                   node to a different one of the alternate transmission paths between the respective source  
19                   node and destination node includes applying a control signal to a switching device  
20                   interposed between the source node and the alternate transmission paths associated with  
21                   the respective source node.

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23       22. (Original) The method of Claim 21 wherein each control signal is applied from a  
24                   memory device associated with the communications bus.

1       23. (New) A communications bus connected between a source node and a destination node,  
2           the communications bus including:  
3           (a) a number of alternate transmission paths extending between the source node and  
4                   the destination node on a common substrate comprising a semiconductor chip;  
5           (b) a source switching arrangement interposed between the source node and the  
6                   alternate transmission paths, the source switching arrangement being operable to  
7                   selectively connect the source node to a selected one of the alternate transmission  
8                   paths and disconnect the source node from each other alternate transmission path;  
9           (c) a destination switching arrangement interposed between the destination node and  
10                  the alternate transmission paths, the destination switching arrangement being  
11                  operable to selectively connect the destination node to the selected one of the  
12                  alternate transmission paths and disconnect the destination node from each other  
13                  alternate transmission path;  
14           (d) test circuitry connected to the source node and destination node for applying a test  
15                  signal to each alternate transmission path at initialization of the communication  
16                  bus and for monitoring the destination node to determine whether the respective  
17                  test signal is properly received at the destination node; and  
18           (e) wherein a receive node and first direction control node are associated with the  
19                  source node, and a send node and second direction control node are associated  
20                  with the destination node;  
21           (f) a send switching arrangement is interposed between the send node and each  
22                  alternate transmission path;  
23           (g) a receive switching arrangement is interposed between each alternate transmission  
24                  path and the receive node;

- 1                   (h) a first direction control switching arrangement is interposed between the first
- 2                   direction control node and a control input of a tri-state driver associated with the
- 3                   source node; and
- 4                   (i) a second direction control switching arrangement is interposed between the
- 5                   second direction control node and a control input of a tri-state driver associated
- 6                   with the send node.

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8       24. (New) The communication bus of claim 23 wherein the test circuitry is configured to  
9                   apply the test signal once only.

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